

**Digital Logic Lab Assignment #4**

1. To verify the operation of derived gates.

**Submitted By**

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Year I / SEM I

017BSCIT014

**Submitted To**

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| --- | --- | --- |
|  | **Signature** | **Remarks** |
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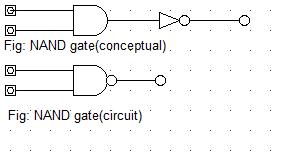
**OBJECTIVE 4.1:**

**TO VERIFY THE OPERATION OF NAND GATE.**

**THEORY:** The NAND gate is a combination of the AND gate with that of an inverter or NOT gate. Here in this gate the output is opposite of the AND gate and output of AND gate is connected to the input of NOT gate.

**Boolean Expression: F=(A.B)’**

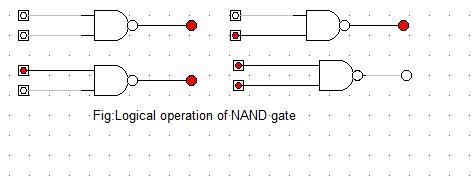
**CIRCUIT DIAGRAM:**

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**TRUTH TABLE:**

|  |  |  |
| --- | --- | --- |
| **INPUT** | | **OUTPUT** |
| **A** | **B** | **(A.B)’** |
| **0** | **0** | **1** |
| **0** | **1** | **1** |
| **1** | **0** | **1** |
| **1** | **1** | **0** |

**OBSERVATION:**



**OBSERVATION TABLE:**

|  |  |  |
| --- | --- | --- |
| **INPUT** | | **OUTPUT** |
| **A** | **B** | **(A.B)’** |
| **0** | **0** | **1** |
| **0** | **1** | **1** |
| **1** | **0** | **1** |
| **1** | **1** | **0** |

**CONCLUSION:**

Hence, the logical operation of NAND gate was verified.

**REFERENCE:**

http://www.electronics-tutorials.ws/logic/logic\_5.html

**OBJECTIVE 4.2:**

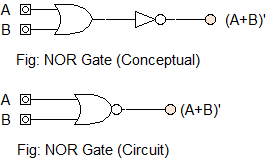
**TO VERIFY THE OPERATION OF NOR GATE.**

**THEORY:**

A NOR gate is a digital logic gate with two or more inputs and one output with behavior that is the opposite of an OR gate. The output of a NOR gate is true all of its inputs are false. If one or more of a NOR gate's inputs are true, then the output of the NOR gate is false.

**Boolean Expression: F=(A+B)’**

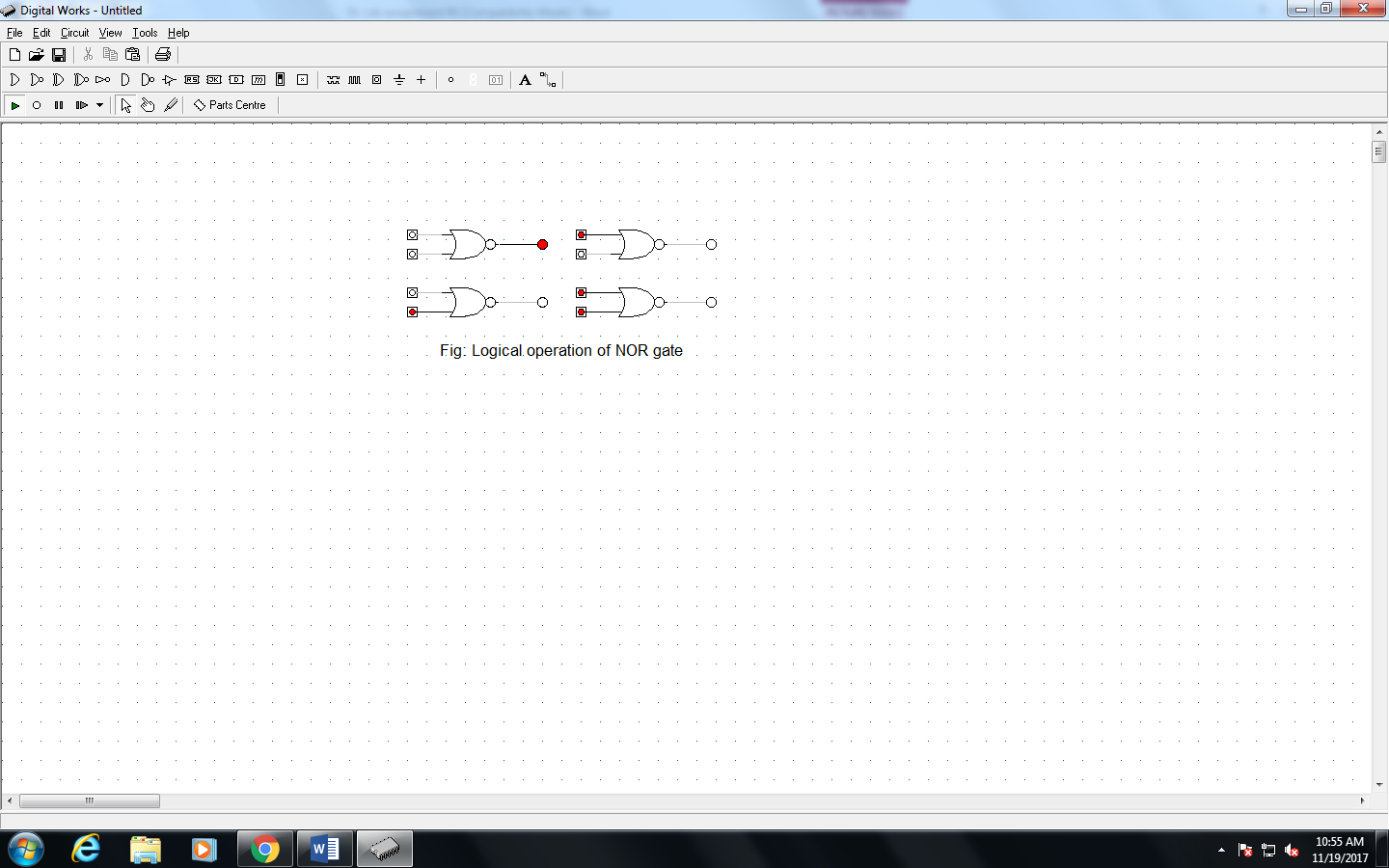
**CIRCUIT DIAGRAM:**



**TRUTH TABLE:**

|  |  |  |
| --- | --- | --- |
| **INPUT** | | **OUTPUT** |
| **A** | **B** | **(A+B)’** |
| **0** | **0** | **1** |
| **0** | **1** | **0** |
| **1** | **0** | **0** |
| **1** | **1** | **0** |

**OBSERVATION:**



**OBSERVATION TABLE:**

|  |  |  |
| --- | --- | --- |
| **INPUT** | | **OUTPUT** |
| **A** | **B** | **(A+B)’** |
| **0** | **0** | **1** |
| **0** | **1** | **0** |
| **1** | **0** | **0** |
| **1** | **1** | **0** |

**CONCLUSION:**

Hence, the logical operation of NOR gate was verified.

**REFERENCE:**

https://logic.ly/lessons/nor-gate/

**OBJECTIVE 4.3:**

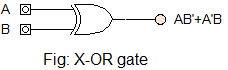
**TO VERIFY THE OPERATION OF X-OR GATE.**

**THEORY:**

An X-OR gate (Exclusive OR gate) is a digital logic gate with two or more inputs and one output that performs exclusive disjunction. The output of an XOR gate is true only when exactly one of its inputs is true. If both of an XOR gate's inputs are false, or if both of its inputs are true, then the output of the XOR gate is false.

**Boolean Expression: F=AB’+A’B**

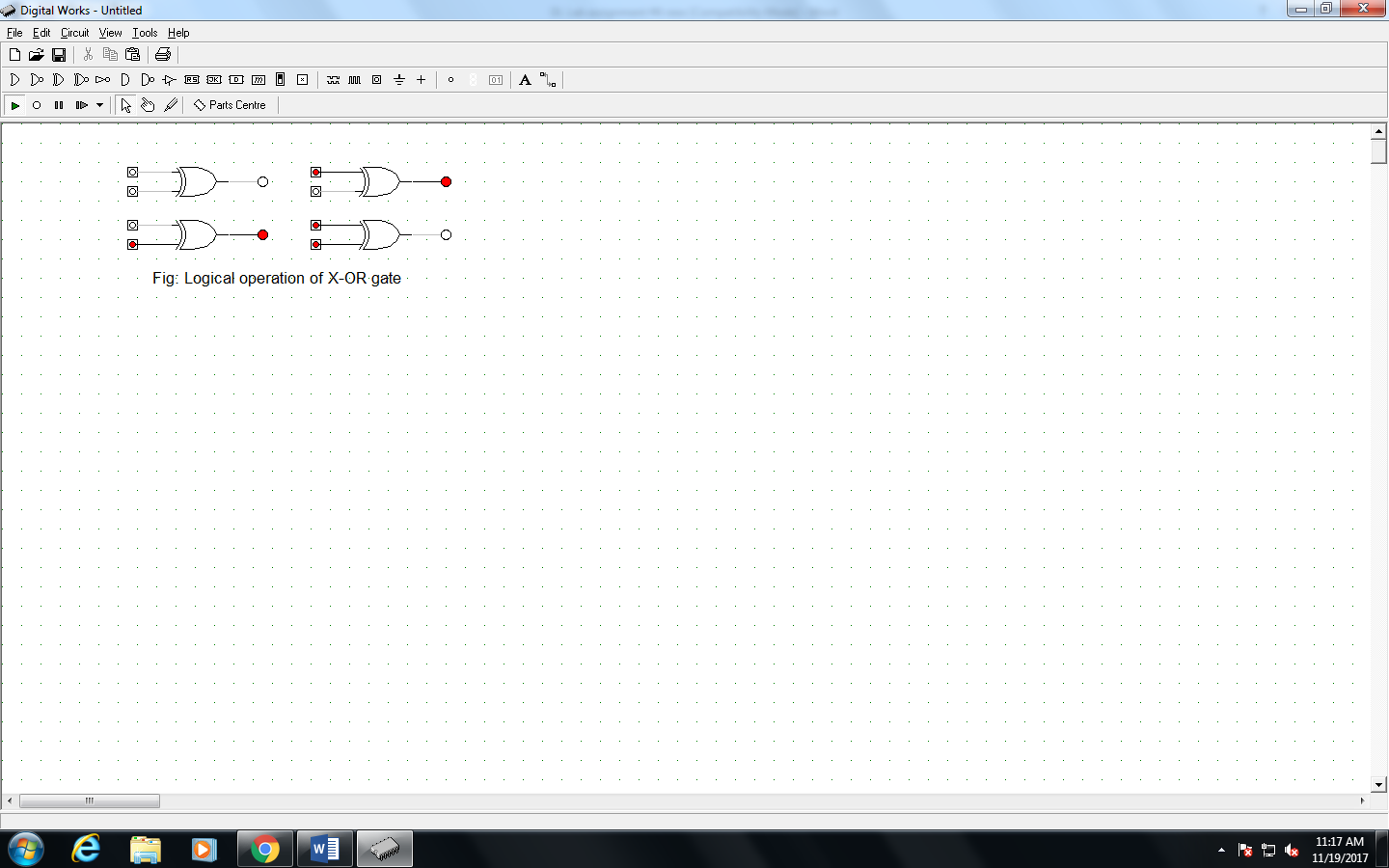
**CIRCUIT DIAGRAM:**



**TRUTH TABLE:**

|  |  |  |
| --- | --- | --- |
| **INPUT** | | **OUTPUT** |
| **A** | **B** | **AB’+A’B** |
| **0** | **0** | **0** |
| **0** | **1** | **1** |
| **1** | **0** | **1** |
| **1** | **1** | **0** |

**OBSERVATION:**



**OBSERVATION TABLE:**

|  |  |  |
| --- | --- | --- |
| **INPUT** | | **OUTPUT** |
| **A** | **B** | **AB’+A’B** |
| **0** | **0** | **0** |
| **0** | **1** | **1** |
| **1** | **0** | **1** |
| **1** | **1** | **0** |

**CONCLUSION:**

Hence, the logical operation of X-OR gate was verified.

**REFERENCE:**

https://logic.ly/lessons/xor-gate/

**OBJECTIVE 4.4:**

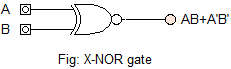
**TO VERIFY THE OPERATION OF X-NOR GATE.**

**THEORY:**

An XNOR gate (Exclusive NOR gate) is a digital logic gate with two or more inputs and one output that performs logical equality. The output of an XNOR gate is true when all of its inputs are true or when all of its inputs are false. If some of its inputs are true and others are false, then the output of the XNOR gate is false.

**Boolean Expression: F=AB+A’B’**

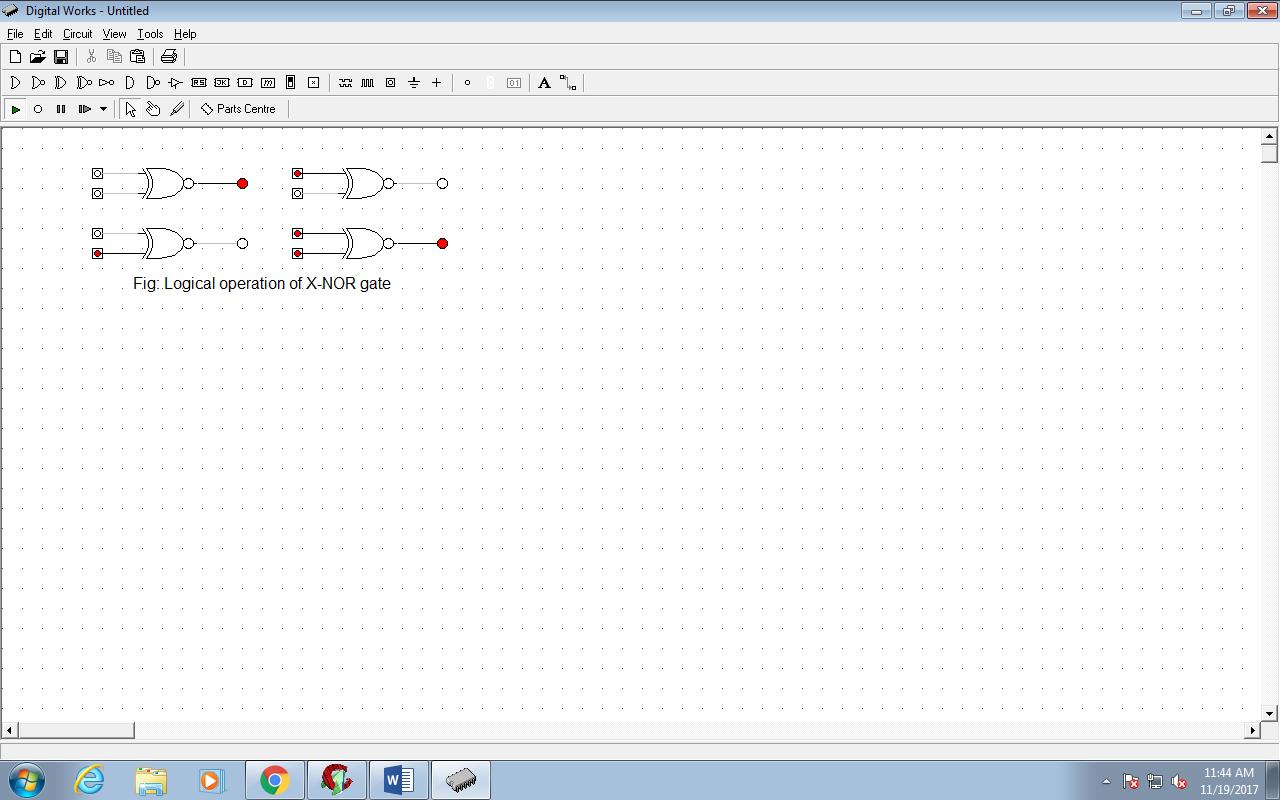
**CIRCUIT DIAGRAM:**



**TRUTH TABLE:**

|  |  |  |
| --- | --- | --- |
| **INPUT** | | **OUTPUT** |
| **A** | **B** | **AB+A’B’** |
| **0** | **0** | **1** |
| **0** | **1** | **0** |
| **1** | **0** | **0** |
| **1** | **1** | **1** |

**OBSERVATION:**



**OBSERVATION TABLE:**

|  |  |  |
| --- | --- | --- |
| **INPUT** | | **OUTPUT** |
| **A** | **B** | **AB+A’B’** |
| **0** | **0** | **1** |
| **0** | **1** | **0** |
| **1** | **0** | **0** |
| **1** | **1** | **1** |

**CONCLUSION:**

Hence, the logical operation of X-NOR gate was verified.

**REFERENCE:**

<https://logic.ly/lessons/xnor-gate/>